

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4520B** **MSI** Dual binary counter

Product specification  
File under Integrated Circuits, IC04

January 1995

# Dual binary counter

# HEF4520B MSI

### DESCRIPTION

The HEF4520B is a dual 4-bit internally synchronous binary counter. The counter has an active HIGH clock input (CP<sub>0</sub>) and an active LOW clock input ( $\overline{CP}_1$ ), buffered outputs from all four bit positions (O<sub>0</sub> to O<sub>3</sub>) and an active HIGH overriding asynchronous master reset input (MR). The counter advances on either the LOW to HIGH transition of the CP<sub>0</sub> input if  $\overline{CP}_1$  is HIGH or the HIGH to

LOW transition of the  $\overline{CP}_1$  input if CP<sub>0</sub> is low. Either CP<sub>0</sub> or  $\overline{CP}_1$  may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on MR resets the counter (O<sub>0</sub> to O<sub>3</sub> = LOW) independent of CP<sub>0</sub>,  $\overline{CP}_1$ . Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

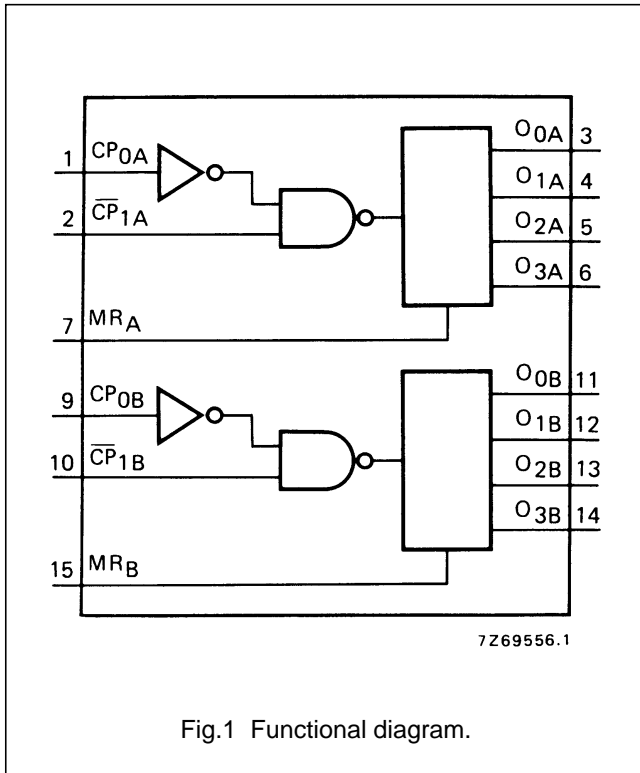
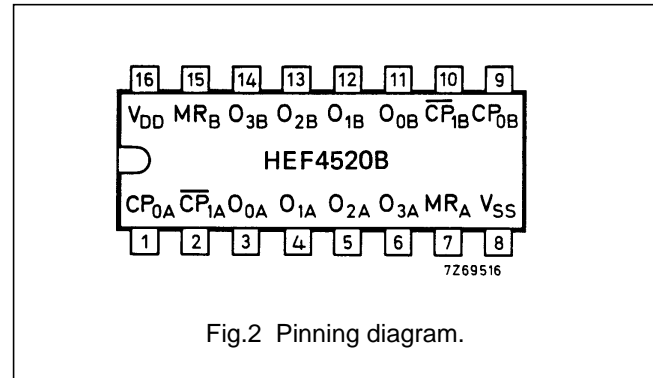


Fig.1 Functional diagram.



- HEF4520BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4520BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4520BT(D): 16-lead SO; plastic (SOT109-1) (SOT109-1)
- ( ): Package Designator North America

### PINNING

- CP<sub>0A</sub>, CP<sub>0B</sub> clock inputs (L to H triggered)
- $\overline{CP}_{1A}$ ,  $\overline{CP}_{1B}$  clock inputs (H to L triggered)
- MR<sub>A</sub>, MR<sub>B</sub> master reset inputs
- O<sub>0A</sub> to O<sub>3A</sub> outputs
- O<sub>0B</sub> to O<sub>3B</sub> outputs

### FAMILY DATA, I<sub>DD</sub> LIMITS category MSI

See Family Specifications

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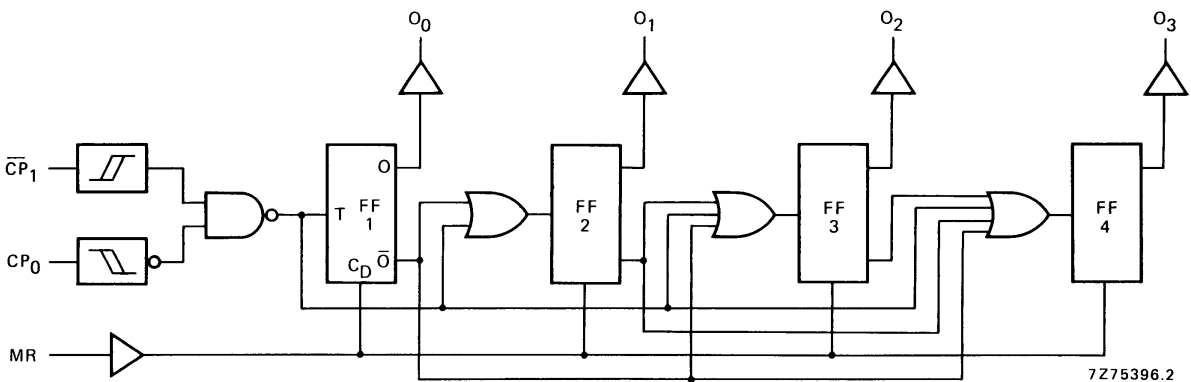


Fig.3 Logic diagram (one counter).

FUNCTION TABLE

| CP <sub>0</sub> | $\overline{CP}_1$ | MR | MODE                                   |
|-----------------|-------------------|----|--|
| ↗               | H                 | L  | counter advances                       |
| L               | ↘                 | L  | counter advances                       |
| ↘               | X                 | L  | no change                              |
| X               | ↗                 | L  | no change                              |
| ↗               | L                 | L  | no change                              |
| H               | ↘                 | L  | no change                              |
| X               | X                 | H  | O <sub>0</sub> to O <sub>3</sub> = LOW |

Notes

- H = HIGH state (the more positive voltage)  
 L = LOW state (the less positive voltage)  
 X = state is immaterial  
 ↗ = positive-going transition  
 ↘ = negative-going transition

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## AC CHARACTERISTICS

 $V_{SS} = 0$  V;  $T_{amb} = 25$  °C;  $C_L = 50$  pF; input transition times  $\leq 20$  ns

|  | $V_{DD}$<br>V                       | SYMBOL     | MIN.      | TYP. | MAX. | TYPICAL EXTRAPOLATION<br>FORMULA           |  |  |
|--|-------------------------------------|------------|-----------|------|------|--|--|--|
| Propagation delays<br>$CP_0, \overline{CP}_1 \rightarrow O_n$<br>HIGH to LOW | 5                                   | $t_{PHL}$  |           | 110  | 220  | ns   | $83 \text{ ns} + (0,55 \text{ ns/pF}) C_L$ |  |
|  | 10                                  |            | 50        | 100  | ns   | $39 \text{ ns} + (0,23 \text{ ns/pF}) C_L$ |  |  |
|  | 15                                  |            | 40        | 80   | ns   | $32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$ |  |  |
|  | LOW to HIGH                         | 5          | $t_{PLH}$ |      | 110  | 220  | ns   | $83 \text{ ns} + (0,55 \text{ ns/pF}) C_L$ |
|  |                                     | 10         |           | 50   | 100  | ns   | $39 \text{ ns} + (0,23 \text{ ns/pF}) C_L$ |  |
|  |                                     | 15         |           | 40   | 80   | ns   | $32 \text{ ns} + (0,16 \text{ ns/pF}) C_L$ |  |
|  | MR $\rightarrow O_n$<br>HIGH to LOW | 5          | $t_{PHL}$ |      | 75   | 150  | ns   | $48 \text{ ns} + (0,55 \text{ ns/pF}) C_L$ |
|  |                                     | 10         |           | 35   | 70   | ns   | $24 \text{ ns} + (0,23 \text{ ns/pF}) C_L$ |  |
|  |                                     | 15         |           | 25   | 50   | ns   | $17 \text{ ns} + (0,16 \text{ ns/pF}) C_L$ |  |
| Output transition<br>times<br>HIGH to LOW                                    | 5                                   | $t_{THL}$  |           | 60   | 120  | ns   | $10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$  |  |
|  | 10                                  |            | 30        | 60   | ns   | $9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$  |  |  |
|  | 15                                  |            | 20        | 40   | ns   | $6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$  |  |  |
|  | LOW to HIGH                         | 5          | $t_{TLH}$ |      | 60   | 120  | ns   | $10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$  |
|  |                                     | 10         |           | 30   | 60   | ns   | $9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$  |  |
|  |                                     | 15         |           | 20   | 40   | ns   | $6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$  |  |
| Minimum $CP_0$<br>pulse width; LOW   | 5                                   | $t_{WCPL}$ | 60        | 30   |      | ns   | see also waveforms<br>Figs 4 and 5         |  |
|  | 10                                  |            | 30        | 15   |      | ns   |  |  |
|  | 15                                  |            | 20        | 10   |      | ns   |  |  |
| Minimum $\overline{CP}_1$<br>pulse width; HIGH                               | 5                                   | $t_{WCPH}$ | 60        | 30   |      | ns   |  |  |
|  | 10                                  |            | 30        | 15   |      | ns   |  |  |
|  | 15                                  |            | 20        | 10   |      | ns   |  |  |
| Minimum MR<br>pulse width; HIGH  | 5                                   | $t_{WMRH}$ | 30        | 15   |      | ns   |  |  |
|  | 10                                  |            | 20        | 10   |      | ns   |  |  |
|  | 15                                  |            | 16        | 8    |      | ns   |  |  |
| Recovery time<br>for MR  | 5                                   | $t_{RMR}$  | 50        | 25   |      | ns   |  |  |
|  | 10                                  |            | 30        | 15   |      | ns   |  |  |
|  | 15                                  |            | 20        | 10   |      | ns   |  |  |
| Set-up times<br>$CP_0 \rightarrow \overline{CP}_1$                           | 5                                   | $t_{su}$   | 50        | 25   |      | ns   |  |  |
|  | 10                                  |            | 30        | 15   |      | ns   |  |  |
|  | 15                                  |            | 20        | 10   |      | ns   |  |  |
| $\overline{CP}_1 \rightarrow CP_0$   | 5                                   | $t_{su}$   | 50        | 25   |      | ns   |  |  |
|  | 10                                  |            | 30        | 15   |      | ns   |  |  |
|  | 15                                  |            | 20        | 10   |      | ns   |  |  |
| Maximum clock<br>pulse frequency   | 5                                   | $f_{max}$  | 8         | 16   |      | MHz  |  |  |
|  | 10                                  |            | 15        | 30   |      | MHz  |  |  |
|  | 15                                  |            | 20        | 40   |      | MHz  |  |  |

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AC CHARACTERISTICS

V<sub>SS</sub> = 0 V; T<sub>amb</sub> = 25 °C; input transition times ≤ 20 ns

|   | V <sub>DD</sub><br>V | TYPICAL FORMULA FOR P (μW)                     |  |
|---|----------------------|--|--|
| Dynamic power dissipation per package (P) | 5                    | $850 f_i + \sum (f_o C_L) \times V_{DD}^2$     | where<br>f <sub>i</sub> = input freq. (MHz)<br>f <sub>o</sub> = output freq. (MHz)<br>C <sub>L</sub> = load capacitance (pF)<br>Σ(f <sub>o</sub> C <sub>L</sub> ) = sum of outputs<br>V <sub>DD</sub> = supply voltage (V) |
|   | 10                   | $3\,800 f_i + \sum (f_o C_L) \times V_{DD}^2$  |  |
|   | 15                   | $10\,200 f_i + \sum (f_o C_L) \times V_{DD}^2$ |  |

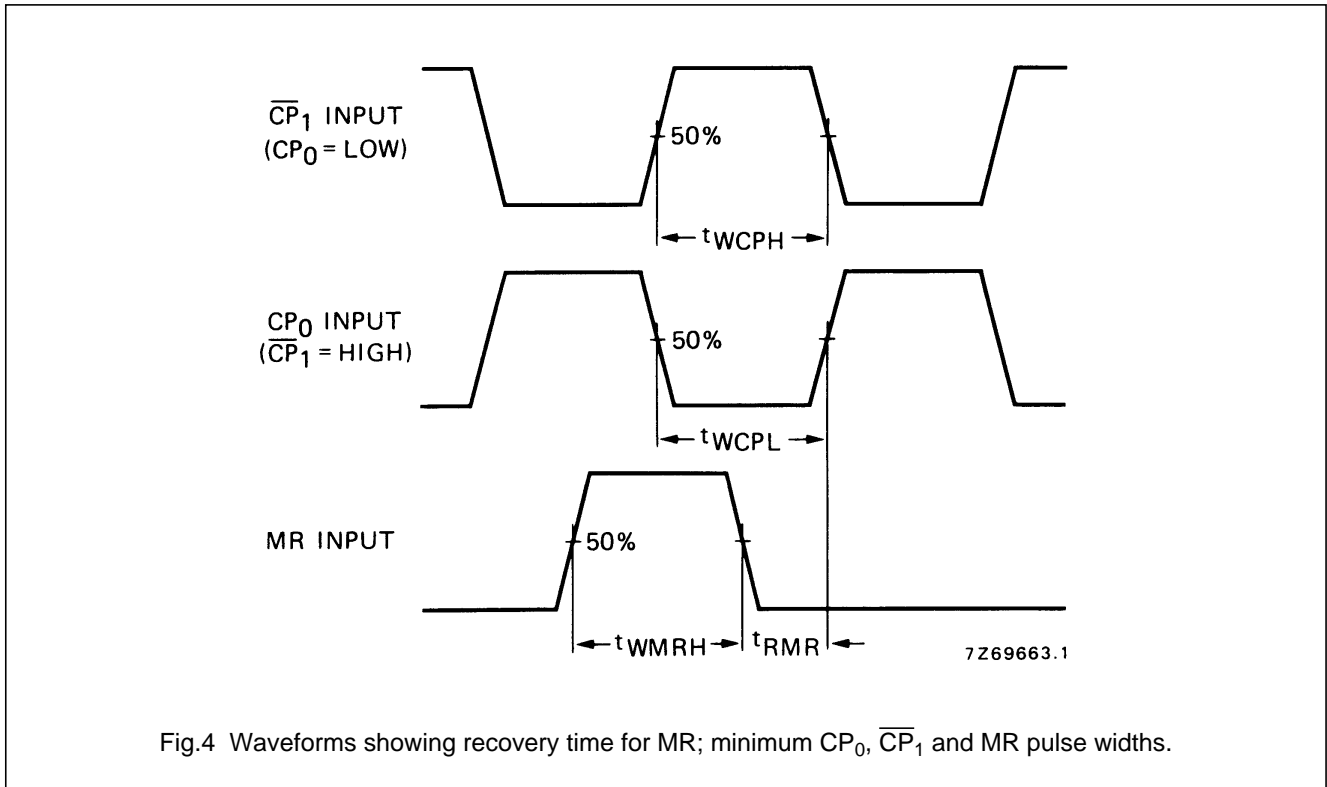


Fig.4 Waveforms showing recovery time for MR; minimum CP<sub>0</sub>, CP<sub>1</sub> and MR pulse widths.

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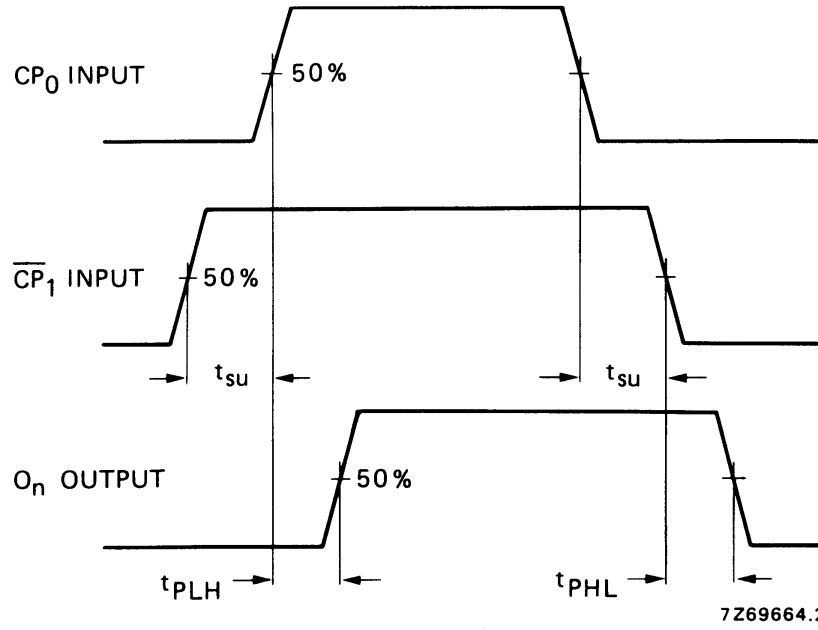


Fig.5 Waveforms showing set-up times for CP<sub>0</sub> to CP<sub>1</sub> and CP<sub>1</sub> to CP<sub>0</sub>, and propagation delays.

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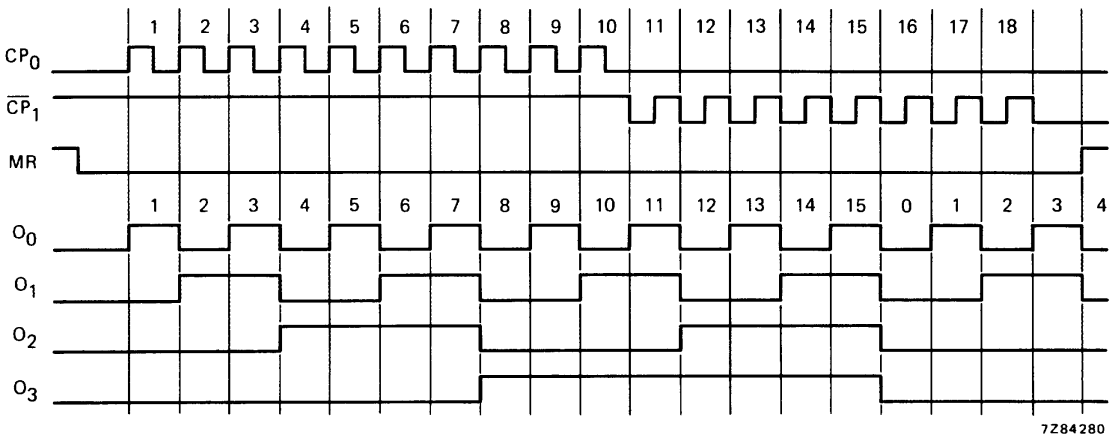


Fig.6 Timing diagram.